REMARKS

The title has been amended to conform to the title of the published application (WO 01/06759).

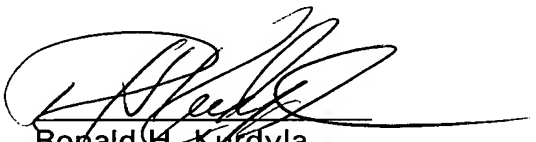
The specification has been amended to include a reference to the priority applications.

The above amendments to the claims have been made to eliminate reference indicia and to meet the requirements of the USPTO. A marked up version is supplied on a separate sheet.

An Abstract is supplied on a separate sheet.

No fee is believed to have been incurred by virtue of this amendment. However, if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832.

Respectfully submitted,
David Glen White et al.



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MARKED UP CLAIMS

What is claimed is:

1. (Amended) In a multiple protocol receiver, a demodulator section, comprising:

a plurality of demodulators [(10(1), 10(2) ... 10(N))]; and

a signal processor [(30)] for processing demodulated data;

[CHARACTERIZED BY] wherein:

the plurality of demodulators [(10(1) ,10(2) ... 10(N))] demodulating data having a respectively different modulation schemes, and each having a tri-state output terminal for demodulated data; and

a signal bus [(20)], coupled between the respective output terminals of the plurality of demodulators [(10(1), 10(2) ... 10(N))], and the signal processor [(30)].

2. (Amended) The demodulator section of claim 1 [CHARACTERIZED BY] wherein a system controller [(40)], coupled to the plurality of demodulators [(10(1) ,10(2) ... 10(N))], for conditioning a selected one of the plurality of demodulators [(10(1), 10(2) ... 10(N))] to pass demodulated data through the output terminal to the signal bus [(20)], and conditioning the other ones of the plurality of demodulators [(10(1), 10(2) ... 10(N))] to exhibit a high impedance at their respective output terminals.

3. (Amended) The demodulator section of claim 1 [CHARACTERIZED IN THAT] wherein each of the plurality of demodulators [(10(1), 10(2) ... 10(N))] comprises a tri-state buffer [(12(1), 12(2) ... 12(N))] having an output terminal coupled to the signal bus [(20)].

4. (Amended) The demodulator section of claim 3 wherein:

the tri-state buffer [(12(1), 12(2) ... 12(N))] in each of the plurality of demodulators [(10(1), 10(2) ... 10(N))] further comprises a control input terminal [(OE)]; and

the demodulator section further comprising a system controller (40), respectively coupled to the control input terminal [(OE)] of the tri-state buffer [(12(1), 12(2) ...

12(N))] in each of the plurality of demodulators [(10(1), 10(2) ... 10(N))], for conditioning the tri-state buffer [(12(1), 12(2) ... 12(N))] in a selected one of the plurality of demodulators [(10(1), 10(2) ... 10(N))] to pass demodulated data through the output terminal to the signal bus [(20)], and conditioning the tri-state buffer [(12(1), 12(2) ... 12(N))] in the other ones of the plurality of demodulators [(10(1), 10(2) ... 10(N))] to exhibit a high impedance at their respective output terminals.

5. (Amended) The demodulator section of claim 4, wherein:

each of the plurality of demodulators [(10(1), 10(2) ... 10(N))] comprises a plurality of tri-state buffers [(12(1), 12(2) ... 12(N))], having their control input terminals coupled in common to the system controller [(40)]; and

the signal bus [(20] comprises a plurality of signal lines [(DATA, CLOCK, PACKET VALID, PACKET DATA)] respectively coupled to the respective output terminals of the plurality of tri-state buffers [(12(1), 12(2) ... 12(N))].

6. (Amended) The demodulator section of claim 4, wherein each of the plurality of demodulators [(10(1), 10(2) ... 10(N))] further comprises a control register [(14(1), 14(2) ... 14(N))], having an input terminal coupled to the system controller [(40)] and an output terminal coupled to the control input terminal [(OE)] of the tri-state buffer [(12(1), 12(2) ... 12(N))].

7. (Amended) The demodulator section of claim 1, wherein a buffer [(25)] coupled between the signal bus [(20)] and the signal processor [(30)].

8. (Amended) The demodulator section of claim 1, wherein the signal processor [(30)] is a transport processor.

9. (Amended) A consumer video receiver, capable of receiving and processing a plurality of video representative signals, comprising:

a plurality of demodulators [(10(1), 10(2) ... 10(N))] for generating respective demodulated video representative signals; and

a controllable transport processor [(30)], for processing a selected one of the demodulated video representative signals, to generate the represented video signal; wherein:

the video representative signals having respectively different data protocols and being modulated using respectively different modulation schemes;

the plurality of demodulators generating the respective demodulated video representative signals having corresponding data protocols, each demodulator having a tri-state output terminal;

the controllable transport processor processing the demodulated video representative signal according to the corresponding data protocol; and

a data bus, coupled between the respective output terminals of the plurality of demodulators and the controllable transport processor.

10. (Amended) The consumer video receiver of claim 9, wherein the controllable transport processor is fabricated on a single integrated circuit [(IC)].

11. (Amended) The consumer video receiver of claim 9, wherein the receiver is contained within a single enclosure.

12. (Amended) The consumer video receiver of claim 9, wherein the respectively different data protocols are selected from the group consisting of direct satellite system [(DSS)] signals, terrestrial broadcast high definition television [(HDTV)] signals, and direct video broadcast [(DVB)] signals.

13. (Amended) The consumer video receiver of claim 9, wherein the respectively different modulation schemes are selected from the group consisting of quadrature phase shift keyed [(QPSK)], vestigial sideband [(VSB)], and quadrature amplitude modulated [(QAM)].